REMARKS

After entry of this Amendment, claims 32-34, 37-66, and 70-89 will be pending. Claim 74 has been amended to correct a typographical error. Claims 67-69 have been cancelled. No new matter has been added. Applicant notes with appreciation the Examiner's allowance of claims 71-76, 80-84, 87, and 88.

Rejection of claims under 35 U.S.C. § 112

Claim 32 is rejected under 35 U.S.C. § 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor, at the time the application was filed, had possession of the claimed invention. Applicant submits that adequate description may be found at least on page 22, lines 11-12, which discloses exemplary channels having a larger Ge concentration than that of an underlying relaxed SiGe layer, i.e., channels having a larger innate lattice constant than that of the underlying relaxed SiGe layer (because Ge has a larger lattice constant than Si) which one of skill in the art would recognize as being compressively strained. Indeed, the fact that such an embodiment exhibits compressive strain is confirmed by the disclosure that a Si layer (or a SiGe layer having a lower Ge concentration) is tensilely strained when provided on a relaxed SiGe layer. *See, e.g.,* Specification, page 2, lines 21-22. Further support appears on page 11, claim 3 of U.S. Provisional Application Serial No. 60/273,112, to which the instant application claims priority. Thus, Applicant submits that the subject matter of claim 32 meets the requirements of 35 U.S.C. § 112.

Rejection of claims under 35 U.S.C. § 103

Claims 39 and 89 are rejected under 35 U.S.C. § 103(a) as being obvious over N. Sugii, et al., "Role of $Si_{1-x}Ge_x$ Buffer Layer on Mobility Enhancement in a Strained-Si n-Channel Metal-Oxide-Semiconductor Field-Effect Transistor," *Appl. Phys. Lett.*, Vol. 75, No. 19, pp. 2948-2950 (1999) ("Sugii") in view of Mizuno et al., "Electron and Hole Mobility Enhancement in Strained-Si MOSFET's on SiGe-on-Insulator Substrates Fabricated by SIMOX Technology," *IEEE Electron Device Letters*, Vol. 21, No. 5 (May 2000) ("Mizuno").

The Examiner relies on Sugii to teach all of the limitations of independent claim 39, except for providing an insulating layer comprising SiO_2 disposed beneath a first strained layer.

The Examiner relies on Mizuno to supply this feature, stating that it would have been obvious to one of ordinary skill in the art to modify the teachings of Sugii with those of Mizuno to form a structure with superior electronic characteristics.

In the Response to Office Action submitted on August 15, 2007 ("the previous Response"), Applicant responded in detail to the identical rejection of claim 39, including a submission of evidence demonstrating that the Examiner's combination of Sugii and Mizuno is improper. The Examiner has not responded to Applicant's evidence, so Applicant herein repeats that portion of the previous Response for the Examiner's convenience and respectfully requests consideration thereof:

> For the reasons that follow, we respectfully submit that the proposed combination would not be made by one of skill in the art, and, furthermore, that the function of Sugii's device is destroyed by the combination with Mizuno. Sugii specifically forms his strained Si-based structures on relaxed $Si_{1-x}Ge_x$, where x is 0.2 or 0.3, corresponding to 20% or 30% Ge. *See* Sugii, p. 2948, paragraph 3. Mizuno forms his structure by implanting oxygen ions into relaxed $Si_{0.9}Ge_{0.1}$ (i.e., 10% Ge) and annealing at 1350 °C. *See* Mizuno, p. 230, section II. Device Structure and Fabrication Processes, paragraph 1. The combination of the structure of Sugii with the method of Mizuno would result in the high temperature annealing of SiGe layers having 20% or 30% Ge at 1350 °C. However, this extreme temperature is higher than the melting point of SiGe alloys containing 20-30% Ge, as expressly shown by the solidus line of the Si-Ge phase diagram. *See* S. K. Ghandi, VLSI Fabrication Principles: Silicon and Gallium Arsenide, John Wiley & Sons, Inc.: New York, p. 74 (1994) [attached to the previous Response as Appendix 1]. The melting point of SiGe alloys containing 20-30% Ge falls between approximately 1200 °C and 1275 °C. Thus, it would not be obvious to one of ordinary skill in the art to apply the method of Mizuno to the structure of Sugii, as layers of Sugii's structure would melt and be rendered inoperative. Notably, Mizuno and his co-workers themselves admitted, in a subsequent publication, that their method is not usable with SiGe having a high Ge content. Mizuno et al. stated that "the melting point of SiGe layers with high Ge content is too low for the high temperature annealing of the SIMOX process," and that the Ge content of layers compatible with the process is limited to be lower than 14%. *See* p. 601, left column, paragraph 3 of T. Mizuno, et al., "Relaxed SiGe-on-Insulator Substrates without Thick SiGe Buffer Layers," Appl. Phys. Lett., Vol. 80, No. 4, pp. 601-603 (2002) [attached to the previous Response as Appendix 2].
>
> Thus, one of ordinary skill in the art would not combine the structures of Sugii with the methods of Mizuno. Therefore, we submit that, for at least these reasons, independent claim 39 and claims depending therefrom are patentable over the cited art.

See the previous Response, page 12.

In rejecting claim 89, the Examiner contends that "Mizuno (page 230, 2nd column) discloses the step of providing an insulator comprises wafer bonding." Applicant submits that Mizuno does not teach or suggest providing an insulator layer by wafer bonding. As disclosed in the instant Specification, wafer bonding is a technique that enables the transfer of a layer from one substrate to another after the two substrates are bonded together. *See* Specification, Figs. 4A-4D and related text. In marked contrast, Mizuno discloses formation of a buried SiO_2 layer inside an $Si_{0.9}Ge_{0.1}$ layer on a single wafer by the Separation-by-Implanted-Oxygen ("SIMOX") technique. *See* Mizuno, p. 230, abstract and right column. Via SIMOX, Mizuno forms his SiO_2 layer by implantation and annealing rather than by wafer bonding, as required by claim 89. Indeed, the process used by Mizuno is vastly different from wafer bonding. Whereas wafer bonding involves physical attachment to a pre-existing layer, Mizuno's process builds that layer internally.

Therefore, we submit that, for these additional reasons, dependent claim 89 is patentable over the cited art.

Rejection of claims under 35 U.S.C. § 102

Claims 67-69 are rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,881,632 to Fitzgerald et al. Applicant submits that this rejection is mooted by the cancellation of claims 67-69.

CONCLUSION

In light of the foregoing, Applicant respectfully submits that all claims are now in condition for allowance.

The Commissioner is hereby authorized to charge the required fee of $810 for the Request for Continued Examination to Deposit Account No. 07-1700. Applicant believes that no additional fees are necessitated by the present Response. However, in the event that any additional fees are due, the Commissioner is hereby authorized to charge any such fees to Deposit Account No. 07-1700.

If the Examiner believes that a telephone conversation with Applicant's agent would expedite allowance of this application, the Examiner is cordially invited to call the undersigned.

Respectfully submitted,

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